

REMARKS

Claims 1-21 are pending in this application.

Claims 11, 15-17 and 20 are objected to.

Claims 1-10, 12-14, 18, 19 and 21 are rejected.

In the Office Action dated 13 March 2002, claims 2-8 and 14 are rejected under 35 USC §112, second paragraph, as being indefinite. Replacement claim 2 above is believed to overcome the '112 rejection of claims 2-8. The undersigned does not understand why claim 14 was rejected and, unfortunately, the office action provides no explanation.

No other rejection of claims 6-8 was made. Therefore, these claims should be either allowed or objected to.

Claims 1-5, 9, 10, 12-14, 18, 19 and 21 are rejected under 35 USC §103(a) as being unpatentable over Richardson et al. alone, Ma et al. alone, and Spree et al. alone. These rejections are respectfully traversed for the reasons that follow.

Independent claims 1, 13 and 21 all recite power conversion by operating a source-side inverter in current mode and a drive-side inverter in a commutation mode. The office action acknowledges that none of the cited documents teach or suggest this combination of control modes. However, the office action states that both control modes are known, and therefore would have been obvious choices for the power conversion.

To properly make the '103 rejection, the examiner must find some teaching, suggestion or incentive in the prior art for combining the operation of a source-side



inverter in current mode with the operation of a drive-side inverter in a commutation mode.

The examiner has offered no reason, motivation or incentive for combining these two control modes; he has simply made a bald conclusion of obviousness. Without any factual basis, how then does the examiner reject the claims? One possibility is that the examiner is engaging in hindsight reconstruction of the claimed invention, using applicants' structure as a template and selecting elements from the cited documents to fill the gaps. However, such hindsight reconstruction does not provide a legal basis for a '103 rejection.

Another possibility is that the examiner is relying on his personal knowledge of power conversion to make the rejection. If this is true, then the examiner is respectfully requested, pursuant to MPEP §707 and 37 CFR §1.104(d)(2), to cite a document or provide an affidavit supporting his personal knowledge about the obviousness of performing power conversion by the *combination* of operating a source-side inverter in current mode and that a drive-side inverter in a commutation mode.

In conclusion, over Richardson et al, Ma et al., and Spree et al. alone and in combination, do not offer a teaching, reason, motivation or incentive for combining the operation of a source-side inverter in current mode with the operation of a drive-side inverter in a commutation mode. Therefore, the '103 rejections over these documents should be withdrawn.

The specification has been amended to correct a typographical error. No new subject matter has been added.

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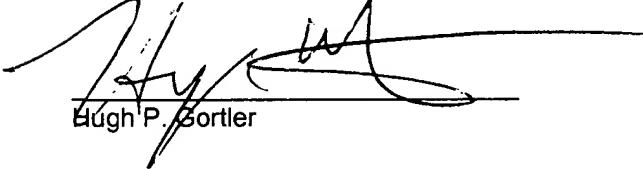
The examiner is respectfully requested to withdrawn the '103 and '112 rejections and issue a notice of allowability. If any issues remain, the examiner is invited to contact the undersigned.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Assistant Commissioner of Patents,
Washington, D.C. 20231 on June 10, 2002.


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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Power flow in the ac-to-ac converter 10 of Figure 1 is uni-directional. However, power flow may be made bi-directional by adding a diode bridge to the dc current link (see Figure 7). This addition enables the source-side inverter 18 to maintain the same current direction with an inverted voltage obtained from the capacitor bank capacitors, while at the same time providing a current reversal on the drive-side inverter 20, while maintaining the same voltage polarity.

IN THE CLAIMS

2. The apparatus of claim 1, wherein the controller commands the source-side inverter to perform current regulation on the dc current link during a first portion of each modulating cycle and current mode space vector modulation during a second portion of each modulating cycle.

